REMARKS

Claims 1-20 were pending in the application when the Office Action was mailed on September 21, 2007. The Office Action rejected claims 1-20. Applicant has amended claims 1, 4, 6, 9, 11, 12, 15, and 18-20; canceled claims 5, 10, 16 and 17; and added claims 21-24. Accordingly, claims 1-4, 6-9, 11-15 and 18-24 are now pending.

The Office Action rejected claims 1-20 under 35 U.S.C. § 102(b) over U.S. Patent No. 6,223,322 ("Michigami"). Applicant respectfully traverse these rejections.

Michigami is directed to techniques for managing how memory is read from an optical disk into buffer memory so that error correction code ("ECC") techniques can be applied quickly. (Michigami, Abstract.) As was the convention prior to Michigami's technique, data was read into the buffer from an optical disk and then the buffer was processed by an ECC processor in column and row directions to detect and correct errors, which resulted in long decoding time. Michigami's technique reads data from an optical disk into memory in an interleaved format. The memory has two physical memory banks: Bank 0 and Bank 1. (See "Physical Mapping" in Michigami, Figure 5, and 6:32-33.) Michigami's Figure 5 illustrates a "Logical Mapping" and a "Physical Mapping." The Logical Mapping illustrates how data blocks are stored in an optical disk. (See Michigami, 6:42-45.) The Physical Mapping illustrates how the data blocks are stored in memory after they are read from the optical disk. (Id.) As data blocks are read from an optical disk, they are alternately stored in the two memory banks. For example, data block A0 is read and then stored in Bank 0; data block B0 is next read and then stored in Bank 1; data block A1 is next read and then stored in Bank 0; and so forth. (Id.) By interleaving the data blocks in this manner, Michigami's technique can operate the memory in an interleaved and pipelined manner for moving the elements of each data array out of a local memory for ECC correction and then back into the local memory after correction. (Michigami, 4:12-15.) Doing so speeds up memory access. The length of blocks that are stored in memory is specified as $Y <= 2^N \times (2m + 1)$, where Y is the number of bytes in each coded data line, N is used to specify the number of

bytes in each row, and m is used to specify the number of blocks. (Michigami, 6:58-7:7.) The variables N and m can be varied to improve use efficiency of the memory. (Michigami, 7:1-7.)

Applicant's technology is directed to improving optical disk performance by using buffer memory more efficiently. Conventionally, a pre-charge operation occurs on a memory bank between accesses by two pipes to the memory bank. (See applicant's Figure 2.) For example, pipe(a) accesses bank 0 at time T0 and then pipe(b) accesses bank 0 at time T1. However, before pipe(b) can access bank 0, that bank must be pre-charged because that is how SDRAM operates. Pre-charges generally take several clock cycles. Applicant's technology causes the pre-charge to occur for a second bank while a first bank is being accessed. Refer to applicant's Figure 6. While pipe(a) accesses bank 0 at time T1, applicant's technology causes bank 1 to be pre-charged so that pipe(b) can access bank 1 at time T2. Applicants' technology functions with any number of memory banks. To do so, applicant's technology computes physical memory addresses based on a block index value and the number of banks (N). (See, e.g., applicant's Figure 4 and paragraphs [0030]-[0033].)

Claims1-4 recite "mapping the block index to a physical address of a memory based on the block index value and a number N, wherein N is a number of banks of the memory." Thus, applicant's technology functions with any number of memory banks. For example, if there are two memory banks, applicant's technology uses N=2; and if there are three memory banks, applicant's technology uses N=3. Michigami does nothing like this. In Michigami, the physical address is based on the logical address. (See, e.g., Michigami, at 9:27-43 and 9:65-10:10:51.) By using applicant's technology, additional memory banks can be added, such as to speed up reading and writing operations. According to the Office Action, Michigami teaches this feature at Figure 5. (Office Action, Page 3.) The Office Action is incorrect. Although Michigami has two banks, there is no indication in either Figure 5 or its corresponding description in Michigami's specification that the physical mapping has anything to do with the bank

number or block index value. The variable "N" in Michigami can be varied even though the number of memory banks does not vary. Because not every element of claim 1 is taught or suggested by the applied references, claim 1 and its dependent claims are allowable.

Claims 6-9 and 11 recite "dividing the block index value by N for acquiring a quotient Q and a remainder R, wherein N is a number of banks of the memory; [and] identifying a physical address based on Q and R." As described above, Michigami has nothing like this. Because not every element of claim 6 is taught or suggested by the applied references, claim 6 and its dependent claims are allowable.

Claims 12-15 recite "means for dividing a value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is a number of banks of the memory; and means for calculating a physical address of the memory in which to store the retrieved block of data based on Q and R." As described above, Michigami has nothing like this. Because not every element of claim 12 is taught or suggested by the applied references, that claim and its dependent claims are allowable.

Claims 18-20 recite "mapping the block indexes sequentially to a plurality of physical addresses of a memory based on the block indexes and a number N, wherein N is a number of banks of the memory wherein the mapping comprises: dividing the block index by N to obtain a quotient Q and a remainder R." As described above, Michigami has nothing like this. Because not every element of claim 20 is taught or suggested by the applied references, that claim and its dependent claims are allowable.

Claims 21-24 are added. Support for the added claims is found in applicant's specification, e.g., at Figures 4 and 6 and their corresponding descriptions in the specification.

The claims each recite a novel combination of elements that is neither taught nor suggested by the applied references and so cannot be properly rejected under either 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a).

Based on these amendments and remarks, applicant respectfully requests early allowance of this application. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-6478.

Payment of $180.00 covering the fee set forth in 37 CFR 1.17(p) and payment for the required fee for a petition for a two-month extension of time is enclosed. Applicant believes no additional fee fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 320528651US1 from which the undersigned is authorized to draw.

Dated: February 21, 2008

Respectfully submitted,

By _____
Rajiv P. Sarathy
Registration No.: 55,592
PERKINS COIE LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000
(206) 359-7198 (Fax)
Attorney for Applicant

Attachments